A New Self-Alignment Technology for Sub-Quarter-Micron-Gate FET's Operating in the *Ka*-Band

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Abstract—**A new self-alignment technology is proposed and applied to GaAs MESFET's. With this technology, sub-quarter-micron gates are fabricated using conventional optical lithography and selective etching of different insulators. Furthermore, an offset gate structure is realized using the self-alignment method. Gate lengths between 340 nm and 90 nm are attained with excellent controllability. This technology is successfully applied to high-power GaAs MESFET's operating in the *Ka*-band. A linear gain of 4.0 dB and a saturation power of 0.8 W are obtained at 28 GHz from an FET with a gate width of 3.6 mm, thus demonstrating the effectiveness of the self-aligned offset gate structure.**

I. Introduction

THE MOST straightforward means for improving the high-frequency performance of FET's is to decrease the gate length and thus reduce the gate–source capacitance. Electron beam lithography [1], [2] and, in some cases, focused ion beam lithography [3] have been adopted to fabricate gates of less than a quarter-micron. For high-power FET's operating at high frequency, however, reducing the gate length alone is not adequate. Power FET's need high breakdown voltage, and therefore usually have an offset gate structure as well as sub-quarter-micron gates.

This paper reports a new self-alignment technology which allows fabrication of gates of less than 100 nm using conventional optical lithography. In addition, an offset gate structure is realized using a self-alignment method. This technology is applied to high-power GaAs MESFET's consisting of many unit FET's. The uniformity of these FET characteristics is checked to show reproducibility. The input–output power characteristics of a MESFET with a 3.6 mm gate width are measured at 28 GHz, thus demonstrating the overall effectiveness of this technology. Furthermore, the smallest achievable gate length is also discussed and it is shown that a 50 nm gate can be fabricated with this technology. As a demonstration of the technology, a MESFET with a 90 nm gate length is fabricated and evaluated at high frequency, and its potential is shown.

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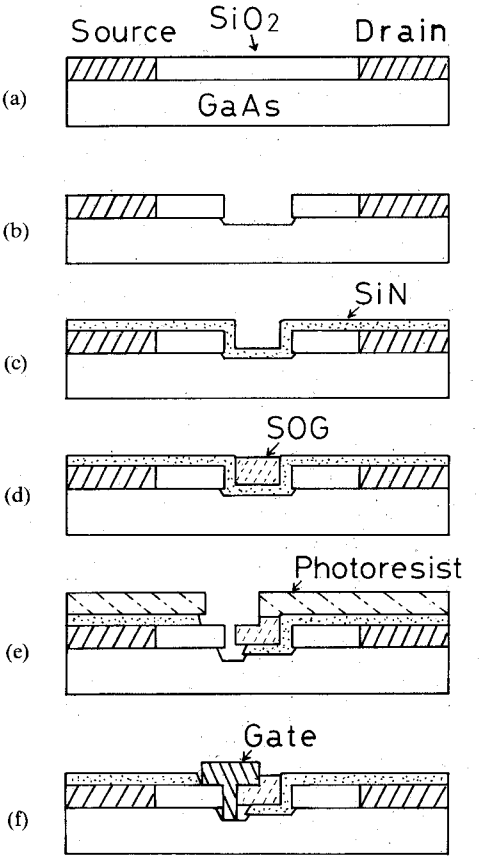

Fig. 1. Fabrication steps in the new self-alignment technology.

II. A New Self-Alignment Technology

The fabrication steps of the self-alignment technology are summarized in Fig. 1. The details are described below.

First, source and drain electrodes as thick as SiO_2 film are formed on the GaAs epitaxial wafer, as shown in Fig. 1(a). Following reactive ion etching (RIE) of the SiO_2 with a CHF_3/C_2F_6 gas mixture, the GaAs first recess structure is formed at the groove in the SiO_2, as shown in Fig. 1(b). Next, SiN film is deposited using plasma-enhanced CVD, as shown in Fig. 1(c). Then the groove is filled with spin-on glass (SOG) by means of ordinary etch-back planarization technology, as shown in Fig. 1(d); i.e., in order to level the whole wafer surface, the wafer coated with

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SOG and baked at 200°C is followed by SOG etch-back technology, until the SiN surface appears. The surface is then covered with photoresist except for the area which includes the SiN sidewall nearer to the source. After selective plasma etching of the SiN sidewall with NF_3 gas, the active layer is etched to form the second recess, as shown in Fig. 1(e). Then the MESFET is completed by depositing and lifting off the gate metal, as shown in Fig. 1(f).

The features of this technology are as follows: (1) The gate length is controlled by the SiN thickness, so that small gate lengths can be fabricated using conventional optical lithography. (2) The cross section of the gate electrode is T-shaped, so that the gate electrode resistance is decreased. (3) The gate electrode is offset nearer to the source electrode using a self-alignment method, so that the drain breakdown voltage is increased [4].

One of the important parameters in this technology is the thickness of the SiN, because it defines the size of the aperture through which the gate metal is deposited. Furthermore, in order to ensure that the aspect ratio of the aperture is appropriate for metallization, the thickness of SiO_2 and the etching ratio between SiN and SOG must be chosen carefully. These factors will be discussed later.

III. Experimental Results

A. Fabrication of Sub-Quarter-Micron-Gate MESFET's

This technology is more effective for high-power FET's operating at high frequency, because gates with both an offset structure and sub-quarter-micron length can be fabricated. Next, the application of such FET's is demonstrated. Fig. 2 is a cross-sectional SEM photograph of a MESFET fabricated with this technology, which is suitable for high-power operation at high frequency. The gate electrode is offset nearer to the source electrode, and the gate length is 200 nm. The distance between source and drain is 3.5 μm. Note that the region between gate and drain is etched in a shallow two-stage recess, compared to a one-stage deep recess in the source–gate region. This asymmetric recess is ideal for achieving high drain breakdown voltage as well as low source–gate resistance. Fig. 3 shows the dc characteristics of the FET. The carrier concentration in the active channel layer was $3.3\times10^{17}\,cm^{-3}$. Although the drain current did not saturate completely, a high transconductance was obtained, e.g. 230 mS/mm when drain and gate were biased at 3 V and 0 V, respectively.

An important factor toward achieving good performance is a high degree of uniformity. An example of a high-power FET is shown in Fig. 4; its total gate width is 3.2 mm and it consists of 32 unit FET's. Good uniformity is indispensable for high gain. As a means of verifying uniformity, the drain current I_d, transconductance g_m, and pinch-off voltage V_p were measured for the 32 unit FET's. The results are shown in Fig. 5. The drain and gate were biased at 3 V and 0 V, respectively, during measurement of I_d and g_m. The numbers on the abscissa indicate the position number of the unit FET's. The dashed lines on the measured points indicate the average of each factor.

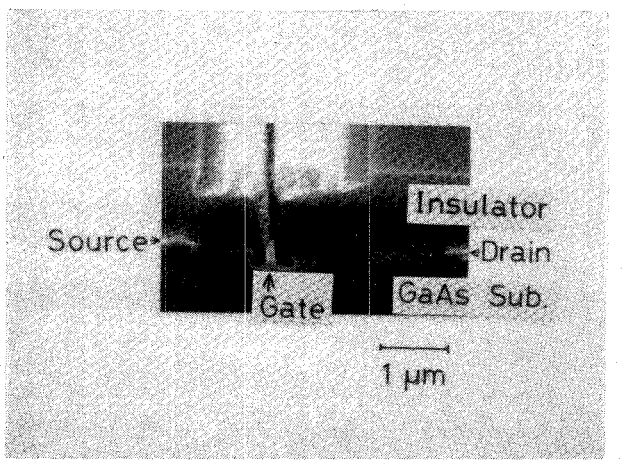

Fig. 2. Cross-sectional SEM photograph of a 200-nm-gate MESFET.

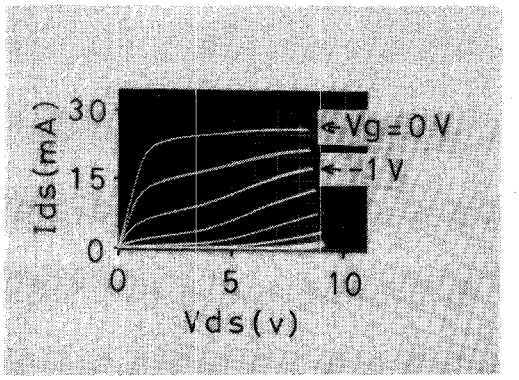

Fig. 3. Drain current–voltage characteristics of the 200-nm-gate MESFET with 75 μm gate width.

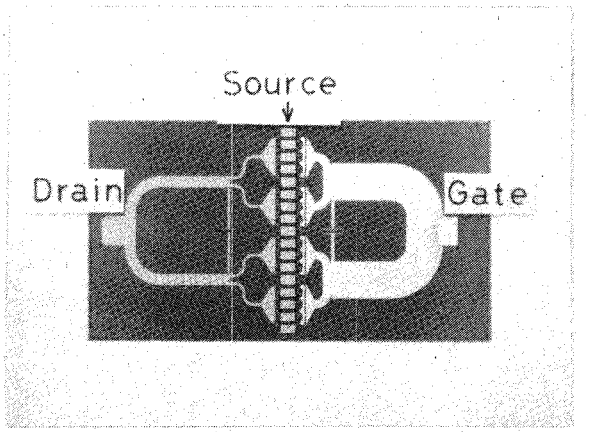

Fig. 4. Top view of a high-power MESFET. RF circuits on gate and drain sides work as power divider and combiner, respectively. Source electrodes are grounded through via holes fabricated under each one.

The three characteristics all showed high uniformity, showing that the high-power FET is suitable for high-power operation. This also demonstrates the excellent reproducibility of the technology. By the way, the variations in I_d and V_p are somewhat larger than that of g_m, and a larger I_d corresponds to a larger V_p. It is reasonable to assume that the variations in I_d and V_p were caused by variations in the recess etching depth, because I_d and V_p

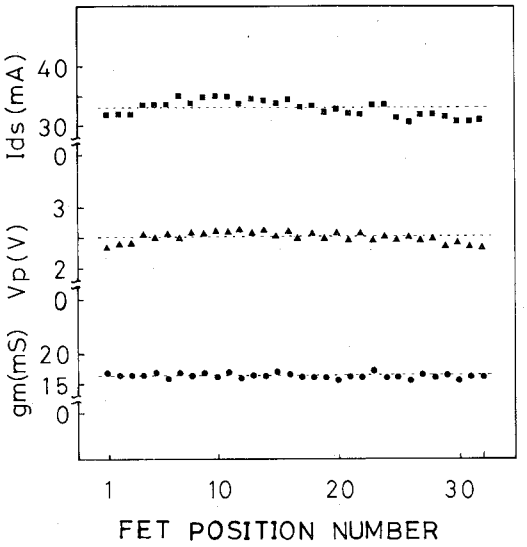

Fig. 5. The dc characteristic distributions of saturation current I_d, pinch-off voltage V_p, and transconductance g_m.

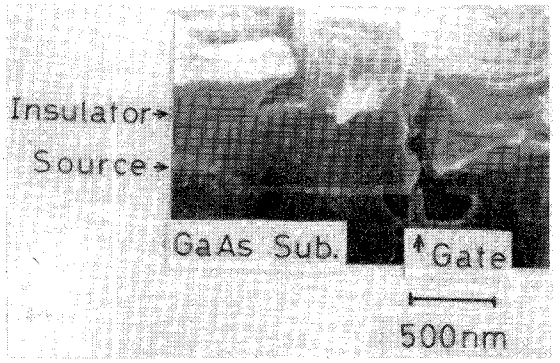

Fig. 6. Cross-sectional SEM photograph of a 90-nm-gate MESFET.

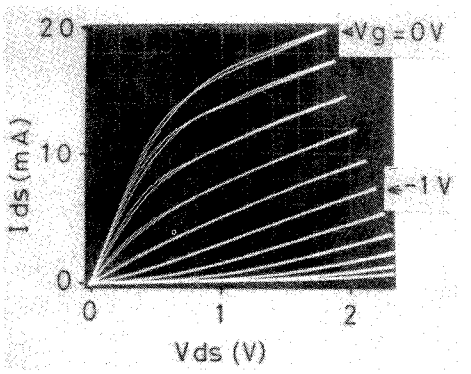

Fig. 7. Drain current–voltage characteristics of the 90-nm-gate MESFET with 75 μm gate width.

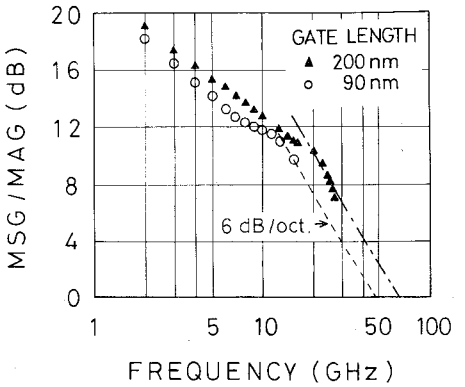

Fig. 8. Small signal RF characteristics of two MESFET's. ○ corresponds to the 90-nm-gate MESFET. During measurement, gate and drain were biased at −0.5 and 3 V, respectively. ▲ corresponds to the 200-nm-gate MESFET. Gate and drain were biased at −0.5 V and 6 V, respectively.

are determined mainly by the thickness and carrier concentration of the active layer, while g_m is determined mainly by the carrier concentration.

Next the characteristics of a MESFET which has the smallest gate length fabricated using this technology are shown. Fig. 6 is a cross-sectional SEM photograph. The active channel layer was fabricated using an MOCVD-grown epitaxial layer with $4.5\times10^{17}\,\mathrm{cm}^{-3}$ carrier concentration. The electrode configurations are the same as in Fig. 2, except for the gate length. The 90 nm gate length was realized in a deep recess. The recess asymmetry was caused by the undercutting of the SiN. Note that the gate metal was deposited fully into the recess in spite of the thick SiO_2 layer of 500 nm.

Drain current–voltage characteristics of this FET are shown in Fig. 7. This shows that drain current does not saturate as well as the 200-nm-gate FET shown in Fig. 3.

B. RF Performance of MESFET's

Small-signal RF characteristics were measured for the two FET's, one with 200 nm gate length and the other with 90 nm gate length. The results are shown in Fig. 8. Gate biases were set at 0.5 V for both FET's, while the drain biases were chosen so that each FET had maximum gain. Their measured upper frequencies were different as a result of the different packages used in the measurement. *MAG*'s were extrapolated by 6 dB degradation per octave. The 90-nm-gate FET showed inferior performance, e.g. 1-dB-lower *MSG* and 3-dB-lower *MAG*, in spite of its smaller gate length. The reason will be discussed later.

Input–output characteristics of a power FET with 3.6 mm gate width were measured at 28 GHz, as shown in Fig. 9. A linear gain of 4.0 dB and a saturation power of 0.8 W (29 dBm) were obtained. These performances are excellent for GaAs MESFET's, thus demonstrating the overall effectiveness of the new technology.

IV. Discussion

A. Smallest Possible Gate Length

In this technology, the gate length is controlled by the SiN thickness, as shown in Fig. 1. Fabricated gate lengths L_g, for various SiN thicknesses T are plotted in Fig. 10. Gate lengths from 340 nm to 90 nm were achieved by depositing SiN of thickness from 550 nm to 160 nm. The good linearity demonstrates the excellent controllability that this technology offers. The ratio of L_g/T is not 1 but

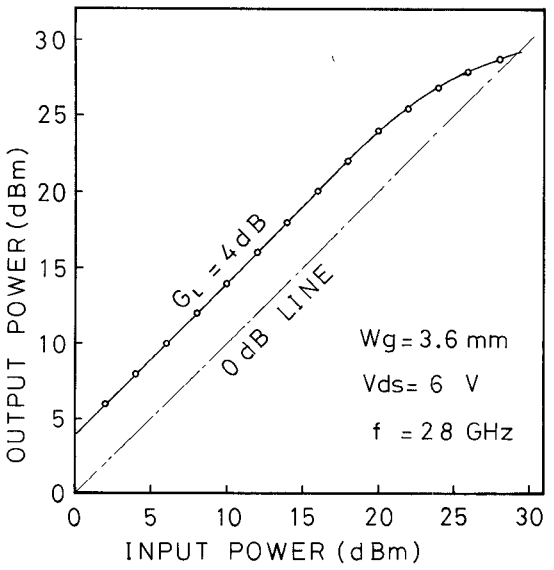

Fig. 9. Input–output power characteristics of a power MESFET.

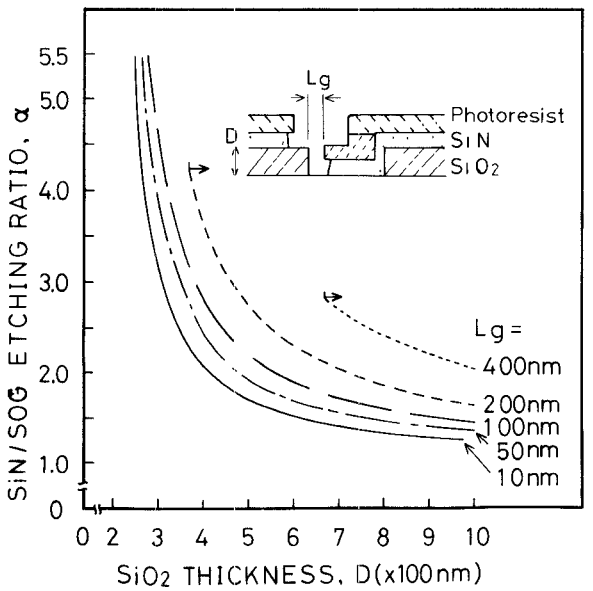

Fig. 11. The relations between SiN/SOG etching ratio, α, and SiO_2 thickness, D, calculated for L_g of 400, 200, 100, 50, and 10 nm.

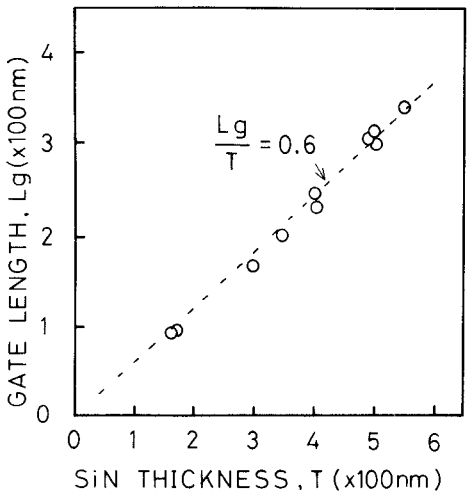

Fig. 10. Gate length, L_g, versus SiN thickness, T.

0.6, due to the characteristic of the SiN step coverage. The factors limiting the gate length will now be clarified and the smallest gate dimension estimated.

The most important parameter is, of course, the SiN thickness, because it determines the aperture size, which is defined by the two sidewalls of SiO_2 and SOG. As shown in Fig. 1, gate metal is deposited through the aperture, which defines the gate length. Next, the aspect ratio of the aperture must be considered. The reasons are the following: the thickness of SiO_2 and SOG must be greater than a certain value in order to maintain a well-defined aperture size, and it must be less than some value to prevent the aperture from closing up during metal deposition, taking the process margin into account. The relations between SiO_2 thickness D, gate length L_g, and etching ratio between SiN and SOG α are determined according to the following equations:

$$\alpha > (D + L_g/0.6)/(D - 200) \tag{1}$$

$$D > L_g/0.6. \tag{2}$$

The results are shown in Fig. 11. Equation (1) is derived from condition (a), which states that SOG is thicker than a certain value (we choose it as 200 nm) so as to keep the cross-sectional shape of the SiO_2 and the SOG at the selective etching of the SiN. Only the SOG thickness is cited because the SOG is etched more and is therefore thinner than SiO_2 in the usual etching condition. Equation (2) is derived from conditions (b) and (c). Condition (b) states that the SOG bottom face is below the SiO_2 top face. Condition (c) states that the ratio L_g/T is always 0.6, as has been shown in Fig. 10, where T is the SiN thickness.

Conditions (a) and (b) are both necessary to define a clear L_g, as shown in the insertion in Fig. 11. Equations (1) and (2) set minima for D and α. The four lines in Fig. 11 show those minima for $L_g = 400$ nm, 200 nm, 100 nm, and 10 nm. A pair of D and α values may be chosen from anywhere in the region above these lines. In the regions for $L_g = 400$ nm and 200 nm, however, the possible values are limited to those larger than the values indicated by ($\rightarrow$). Here the aspect ratio D/L_g is considered. As long as conventional evaporation equipment is used for the gate metallization, the maximum acceptable aspect ratio will be about 6. For example, the aspect ratio of the FET with a 90 nm gate length was 5.5, as calculated from $D = 500$ nm and $L_g = 90$ nm.

From these considerations we have concluded that a 50 nm gate with an aspect ratio of 6 for $D = 300$ nm is the lower limit for a practically achievable gate length with this technique.

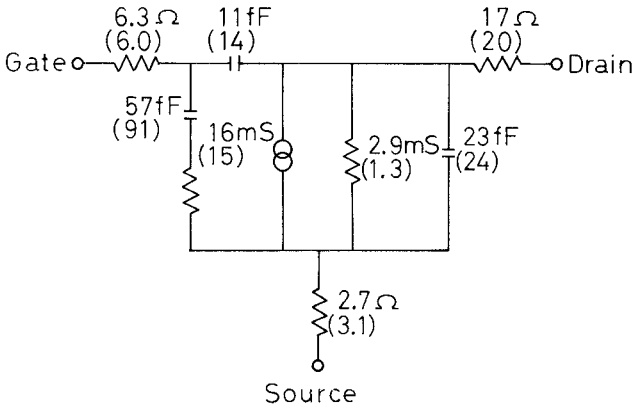

Fig. 12. Equivalent circuit of a 90-nm-gate MESFET. Figures in parentheses correspond to a 200-nm-gate MESFET. Gate widths of both MESFET's are 75 μm.

B. Effects of Reducing the Gate Length

Here we discuss the characteristic differences between FET's with 90 nm and 200 nm gate lengths. As shown in Fig. 8, the RF characteristics of the 90-nm-gate FET are inferior to those of the 200-nm-gate FET. To clarify the reason, equivalent circuits were obtained for the two FET's as shown in Fig. 12. All the capacitances, transconductances g_m, and drain conductances g_d were calculated from the S parameters measured at 500 MHz. On the other hand, resistances were obtained from the forward gate current measurement [5]. Drain and gate were biased at the same values as in *MAG* measurement.

The g_d of the 90-nm-gate FET is more than twice that of the 200-nm-gate FET, while its g_m is not much larger than that of the 200-nm-gate FET in spite of the higher carrier concentration. The gate capacitance of the 90-nm-gate FET is smaller than that of the 200-nm-gate FET because of the reduction in gate length. However, the resistances of the two FET's are almost the same. In particular, both gate resistances are very small in spite of the small gate lengths. For example, the gate resistance of the 90 nm gate, 6.3 Ω, is about one fifth of the value calculated by putting $L_g = 90$ nm into the commonly used equation [6]

$$R_g = \rho z/(3L_g h) \tag{3}$$

where ρ is the specific resistivity (5.0×10^{-6} Ω·cm for thin aluminum), h is the thickness of the deposited gate metal (400 nm), and z is the gate width (75 μm). This demonstrates that the T-shaped gate dramatically reduces gate resistance.

The above comparison shows that the most distinct difference between the two FET's is the drain conductance. This also suggests that the lower *MAG* of the 90-nm-gate FET is caused by the large drain conductance. One of the reasons for the large g_d of the 90-nm-gate FET is the small L_g/d ratio, in which d is the active layer thickness. A ratio larger than 3 is necessary for saturation of the drain current. In the 90-nm-gate FET, however, the thickness of the active layer is 60 nm, as determined by $C-V$ profile measurement, while the gate length is 90 nm. Consequently, the L_g/d ratio was only 1.5. Therefore, a thinner active layer with a higher carrier concentration should be chosen. Furthermore, improvement of the buffer layer is also very important. This can be achieved by, for example, introducing an AlGaAs heterostructure layer.

According to our estimation, when the g_d of the 90-nm-gate FET is decreased to half that of the present value (i.e., as small as that of the 200-nm-gate FET), maintaining other parameters the same, its *MAG* will be improved by 3.0 dB. Furthermore, the improvement of g_d will automatically increase g_m, as suggested by the dc characteristics. We expect the increase in *MAG* to be over 1 dB. Therefore, when g_d is improved, the *MAG* of the 90-nm-gate FET will exceed that of the 200-nm-gate FET.

V. Conclusion

A new self-alignment technology was developed and applied to GaAs MESFET's. Gate lengths of 340 nm to 90 nm were fabricated using conventional optical lithography, and it was shown that gate lengths as small as 50 nm could be realized. This technology was successfully applied to high-power MESFET's. The self-aligned offset gate structure also enabled high gain and high breakdown voltage to be obtained. From a MESFET with a 3.6 mm gate width, a linear gain of 4.0 dB and a saturation power of 0.8 W were achieved, thus demonstrating the effectiveness of this technology. Furthermore, a 90-nm-gate FET was fabricated and evaluated for dc and RF characteristics. Its performance was somewhat inferior to what was expected, but it could have potential if the drain conductance is reduced.

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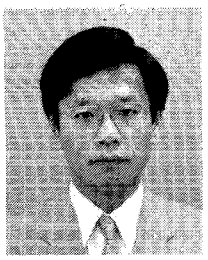

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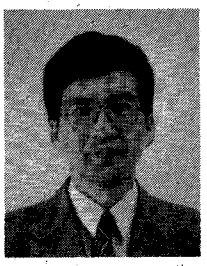

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